Suspended single-electron transistors: fabrication and measurement

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We have fabricated aluminum single-electron transistors in which the island is not in contact with the substrate. This new type of device, which can be called suspended single-electron transistor (SUSET), displayed well-defined I-V and dI/dV-V features typical for high-quality standard SET's.

The single-electron transistor (SET), a device proposed by Averin and Likharev in 1986 and first built by Fulton and Dolan in the next year [1], consists of a small metalic island connected to two leads (electrodes) by two tunnel junctions. The device is controlled through the voltage applied on a gate electrode capacitively coupled to the island.

The SET was proposed for a variety of applications, including counting electrons directly for a capacitance standard [2], direct measurements of single electron tunneling and co-tunneling, Bloch oscillations [3], and microwave photon detection [4]. There has been a lot of interest recently in the use of this device or relatively similar ones as quantum bits for a solid-state quantum computer [5] or as read-out systems for quantum circuits [6]. Finally, multiple-island devices such as Cooper pair pumps and single-electron turnstiles could find applications as metrological standards for current [7] or for measuring decoherence times in nanoscale superconducting systems [8].

The Hamiltonian of an SET contains typically two parts: a tunneling Hamiltonian and a charge Hamiltonian. The first one can be either single-electron tunneling, if the SET is operated in the normal regime, or Josephson tunneling, in the case of a superconducting SET (Cooper-pair transistor). The charge Hamiltonian is given by the total energy associated with the electrostatic energy of the island plus the work done by sources to move the charge around the circuit. This energy contains also a phenomenological quantity usually called "offset charge", which brings an extra contribution to the energy even at zero voltages applied. This quantity takes different values for each device and cooldown and it fluctuates in time with an $1/f$ spectral density.

This effect limitates dramatically the usefulness of the device in many applications, for example it is the main constraining factor for the sensitivity of low-frequency SET electrometers (currently of the order of $\times 10^{-5} e/\sqrt{Hz}$ [10]); the r.f.-SET improves this figure by paying the price of going up to higher frequencies, thus making the device more difficult to operate.

It is believed [11] that this phenomenon is caused by the trapped charge fluctuators in the oxide junction and the substrate; further careful investigations have led to the conclusion that the noise coming from the substrate dominates [12].

One idea to overcome these problems would be to try diferent substrates than the usual SiO_2; indeed, the ex-

isting noise measurements in SET's seem to suggest that there is a correlation between the type of substrate used and the minimum sensitivity achieved. This paper proposes a more radical approach to this issue: to eliminate the substrate itself. We demonstrate that it is indeed possible to fabricate working high-quality devices Al superconducting SET's in which the island is not in contact with the substrate.

Although related free-standing structures have been fabricated before, most notably with semiconducting and metallic nanowires and carbon nanotubes [13], active devices such as superconducting transistors have been available only on membranes or other types of specially designed supports. Besides immediate applications for present mesoscopic electrical circuits requiring low levels of substrate noise, one can speculate that these devices are relevant for building future hybrid solid state - atom (ion) systems which were recently proposed in the context of quantum computing [14].
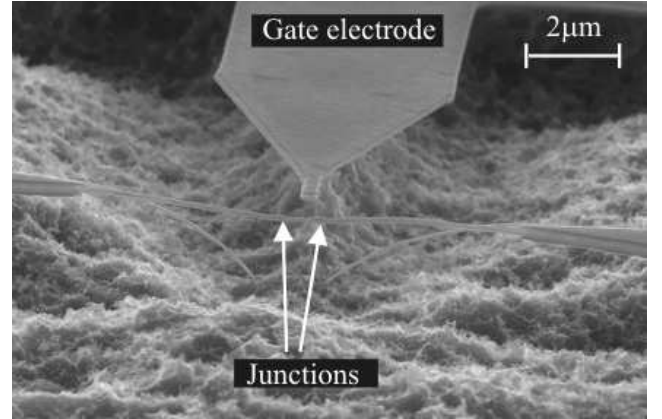

FIG. 1: High-magnification SEM image of an Al SUSET. The tip of the gate electrode (center up) points to the island. The junctions are barely visible in this picture as two thicker nodular structures along the suspended aluminum wire. The two lines starting from the left and right electrodes and pointing downwards (toward the substrate) are the usual by-product of two-angle evaporation.

The suspended Al SET was fabricated using conventional two-angle evaporation on a nitridized Si wafer of 300 nm thickness followed by reactive ion etching. A double layer resist of PMMA-P(MMA-MAA) was spinned on the top of the SiN_2 substrate and baked at 160°C for 45 min (the bottom layer) and 60 min (the upper one). The

resulting thicknesses of the PMMA and P(MMA-MAA) were approximately 250 nm and 350 nm, respectively. The mask was drawn using a scanning electron microscope (JEOL, JSM 840A) with acceleration voltage of 20 kV. The minimum width of the pattern in the island region was 50 nm; after the whole process, the thickness of the metalic wires increased to 100 nm. Then the resists were developed in a mixed solution (1:2) of methyl-*iso*-butylketon (MIBK) alcohol with isopropanol for about 30 s (the upper layer of PMMA) followed immediately by rinsing in isopropylic alcohol, and then in a mixture (1:2) of methyl glycol and methanol for roughly 8 s (the lower layer of P(MMA-MAA)). The chip was further cleaned in a reactive ion etcher (AXIC BENCHMARK) at 30 mTorr pressure with 50 sccm flow of O_2 and 48 W RF-power for 30 s, a process that removes the resist leftovers from the SiN_2 surfaces. The aluminum was evaporated in an UHV chamber at pressure of 2–4×10^{-8} mbar with an evaporation rate of 0.5 nm/s for both the island and the electrodes. The film, with a thickness of 40 nm, was then oxidized in a steady flow of O_2, at a pressure of 20 mbar for three minutes. The junctions were formed by depositing another layer of 60 nm Al at a different angle. In the sample presented here, the 40 nm and 60 nm correspond to the island and the leads, respectively. The process was completed by lift-off, with the sample being slowly heated in acetone up to the boiling point (56°C).

Finally the SET was put into a RIE (AXIC BENCH-MARK) and etched in a two step process. The power was 10% (60 Watts), and the flow of O_2 and CF_4 was 10 % (5 sccm) and 50% (10.5 sccm) respectively. The first step was anisotropic etch at a pressure of 40 mTorr for 3 minutes (ion bombardment to break the surface of the nitride). The second step (isotropic etch) was at a pressure of 70 mTorr for 7 minutes.

The resulting structure is shown in Fig. 1 and Fig. 2. The length of the island is about 1μm, and the thickness is approximately 100 nm.

The SUSET was measured in an electrically shielded room using a Nanoway PDR-50 dilution refrigerator with the lines filtered with commercial π-filters at 4.2 K and a combination of π-filters and RC-filters at room temperature. The conductance was measured using a lock-in amplifier technique. The results are presented in Fig. 3. The sample presented here had a room-temperature resistance $R_n = 73$kΩ.

From the threshold voltage of the quasiparticle branch at 0.755 meV we can determine the gap of Al ($\Delta_{Al} = 0.189$ meV). The charging energy of the sample was derived from the Coulomb-blockade conductance measured at 4.2 K; we found a change in the zero-bias conductance peak $\delta G/G_T = 1.24\%$, yielding a charging energy $E_c = e^2/2C_\Sigma = 13.5\mu$eV, where $C_\Sigma = C_1 + C_2 + C_g$ is the usual definition for the total capacitance of the island.

The critical Josephson current from Fig. 3 is approximately 70 pA; switching-current measurements, which are more precise, gave a value $I_c = 61$ pA for this sample. This corresponds to a quite small Josephson energy
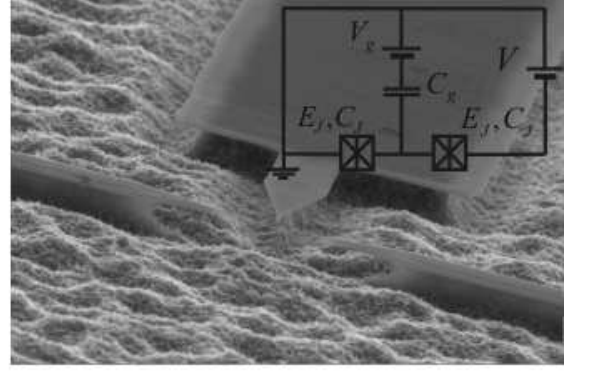

FIG. 2: A lower-magnification SEM picture of a suspended single-electron transistor, showing the effect of etching on the SiN_2 substrate. The structure doesn't touch the resist for a length of about 20 μm. The inset in the upper right corner shows the full large-scale structure, including the bonding pad for the gate.
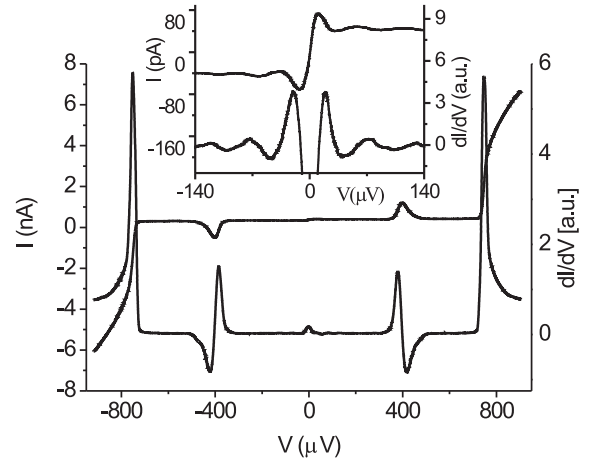

FIG. 3: Current and conductance as function of bias voltage, showing clearly the defining features of a good-quality SET (Josephson current, JQP, and quasiparticle conductance peak). The inset is a low-bias voltage detail, with a better visible Josephson effect and mild Cooper pair resonant peaks in the current.

$E_J = \hbar I_c/2e = 0.13\mu$ eV. The Ambegaokar-Baratoff formula $E_J = R_K \Delta_{Al}/8R_n$, where $R_K = h/e^2 = 25.8$kΩ is the quanta of resistance (von Klitzing constant), yields 8.3μ eV, significantly larger than the measured value. These are a well-known discrepancies for small-junction superconducting SET's, caused by the sensitivity of the Josephson effect for small junctions to the external electromagnetic environment [15]. They occur when E_c is larger or of the same order of magnitude as E_J (therefore the phase of the island is not a good quantum number and the current has strong fluctuations), which is indeed
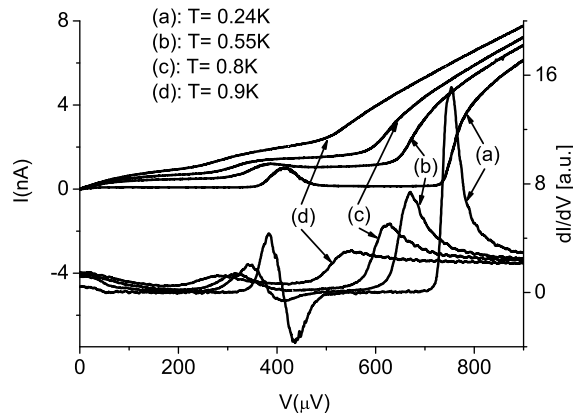
FIG. 4: I-V characteristics as a function of temperature. The sharpest features correspond to T = 0.2 mK; the temperature was then raised close to the critical temperature of Al.

the case for our sample.

In Fig. 3 the two symmetric peaks in the current are due to a combined Josephson and quasiparticle (JQP) tunneling in the junctions; this effect is predicted to happen at a bias voltage $2\Delta_{Al} + E_C \leq eV \leq 2\Delta_{Al} + 3E_C$ [16]. For our sample, this gives 0.391 meV $\lesssim eV \lesssim 0.418$ meV, in excellent agreement with the position of the peak in the experimental data. The JQP features are quite broad, as

expected from the theory of this process for samples with small E_c/Δ [17].

Finally, a measurement at low bias voltages (inset of Fig. 3) reveals a finer structure of resonances in the current, corresponding to oscillations in the conductance. According to the theory of resonant tunneling of Cooper pairs [18], the spacing between consecutive peaks peaks should be $4E_C$, i.e. $54\ \mu$eV. Although the data were quite noisy, it was still possible to estimate the distance between peaks as being indeed 50-60 μeV.

The SUSET is affected by temperature in the same way as conventional SET's. Fig. 4 presents I-V measurements from 0.2 K to about 0.9 K, close to the critical temperature of Al. The low-temperature features get more rounded and they are displaced towards lower bias voltages, in agreement with the decrease of the gap of Al.

In conclusion, we have fabricated and measured a suspended SET. We did not observe any decrease in the quality of the device due to the extra etching process. Therefore, we believe that this new device can be useful in applications that require a precise control of the island charging as well as for investigations of the origin of the noise in single-electron transistors.

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